



PQMD12

NPN/PNP resistor-equipped transistors;
R1 = 47 k Ω , R2 = 47 k Ω

24 July 2013

Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistors (RET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Low package height of 0.37 mm
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications
- Mobile applications

4. Quick reference data

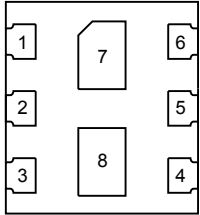
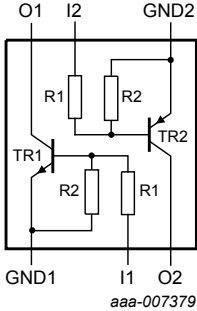
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
Per transistor; for the PNP transistor with negative polarity						
R1	resistance 1	T _{amb} = 25 °C	33	47	61	k Ω
R2/R1	resistance ratio		0.8	1	1.2	



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>Transparent top view DFN1010B-6 (SOT1216)</p>	 <p>aaa-007379</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PQMD12	DFN1010B-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

7. Marking

Table 4. Marking codes

Type number	Marking code
PQMD12	11 00 00

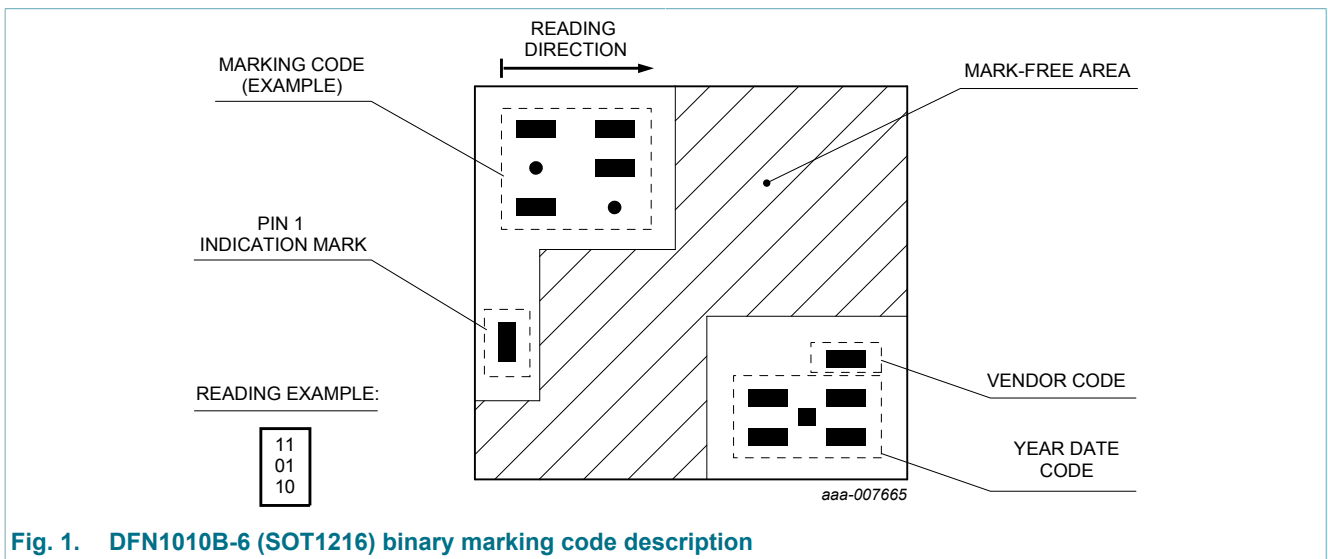


Fig. 1. DFN1010B-6 (SOT1216) binary marking code description

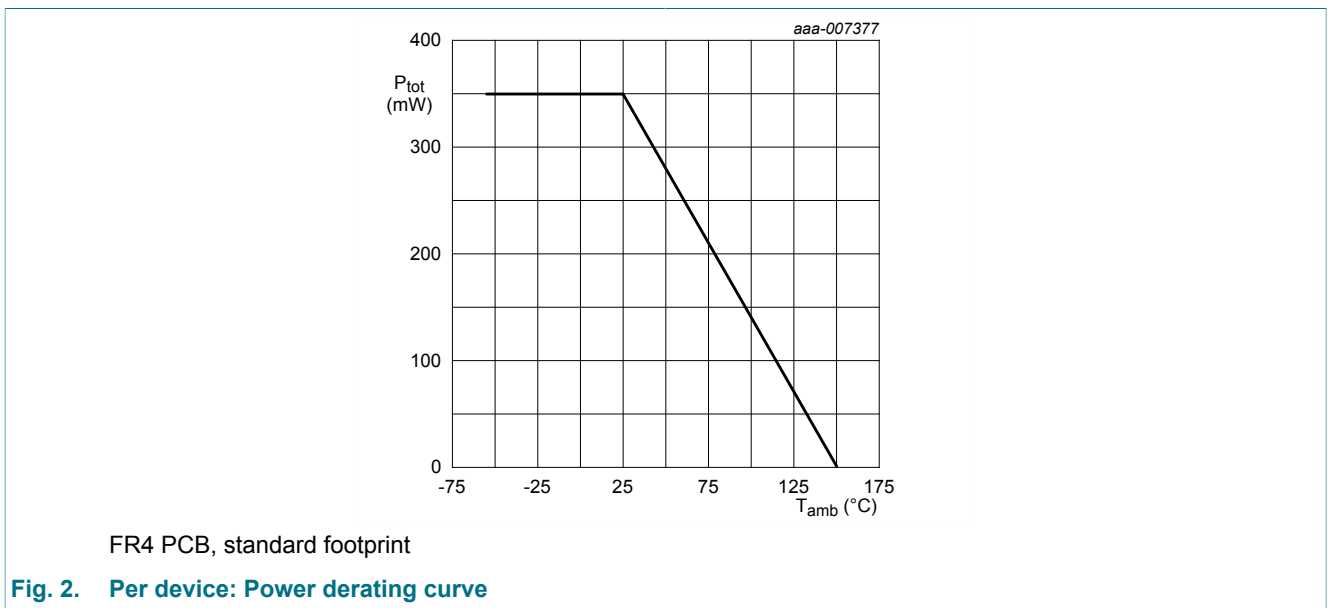
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage	TR1; positive		-	40	V
		TR1; negative		-	-10	V
		TR2; positive		-	10	V
		TR2; negative		-	-40	V
I _O	output current			-	100	mA
I _{CM}	peak collector current	t _p ≤ 1 ms; single pulse;		-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	230	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	350	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

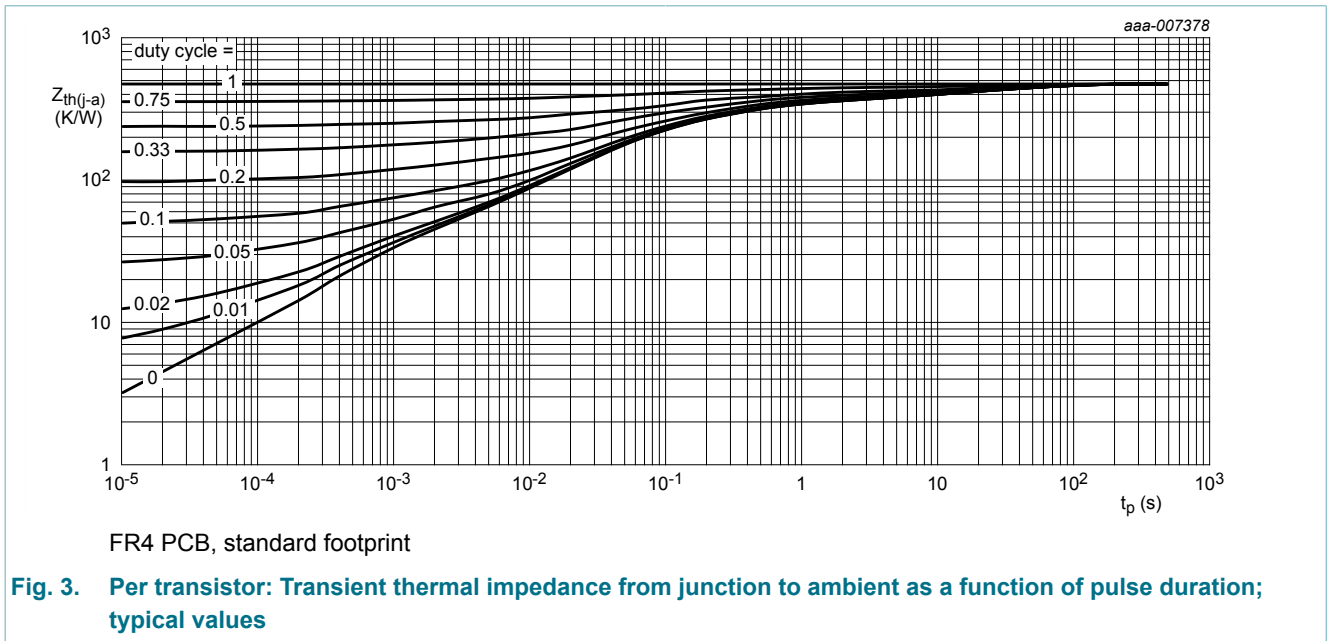


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	543 K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	357 K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



10. Characteristics

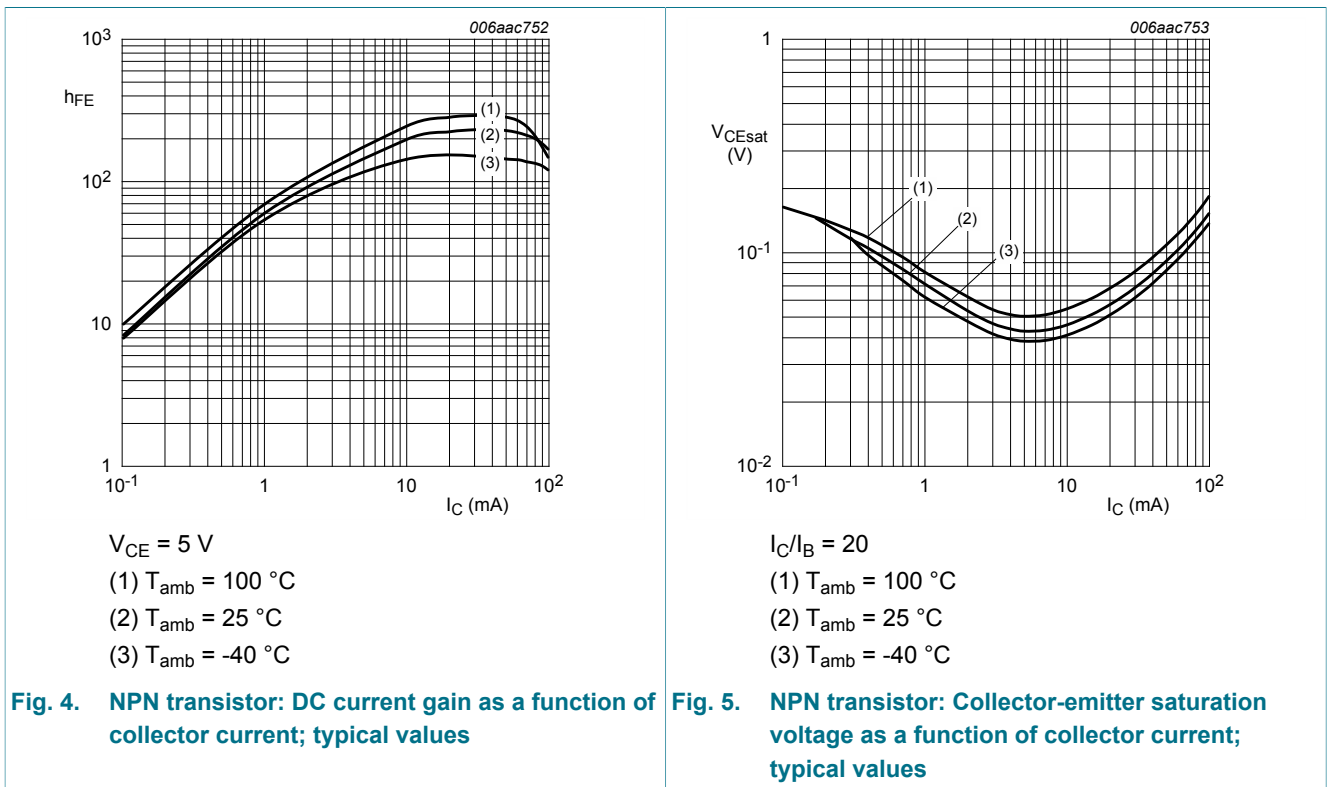
Table 7. Characteristics

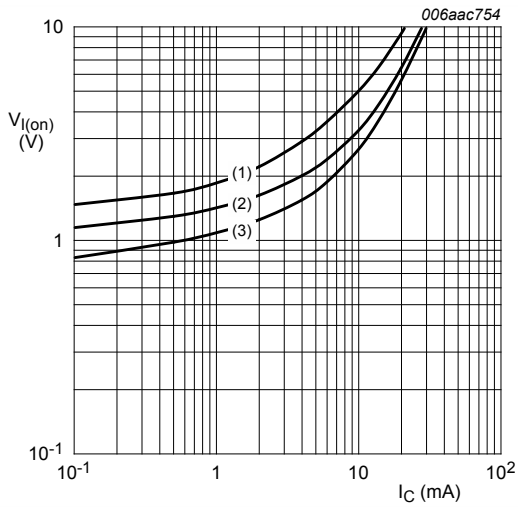
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_{amb} = 150\text{ °C}$	-	-	5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	90	μA

NPN/PNP resistor-equipped transistors; R1 = 47 kΩ, R2 = 47 kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	80	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}; T_{amb} = 25\text{ }^\circ\text{C}$	-	1.2	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 2\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	3	1.6	-	V	
R1	resistance 1	$T_{amb} = 25\text{ }^\circ\text{C}$	33	47	61	kΩ	
R2/R1	resistance ratio		0.8	1	1.2		
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}; \text{TR1 (NPN)}$	-	-	2.5	pF	
		$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}; \text{TR2 (PNP)}$	-	-	3	pF	
f_T	transition frequency	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}; \text{TR1 (NPN)}$	[1]	-	230	-	MHz
		$V_{CE} = -5\text{ V}; I_C = -10\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}; \text{TR2 (PNP)}$	[1]	-	180	-	MHz

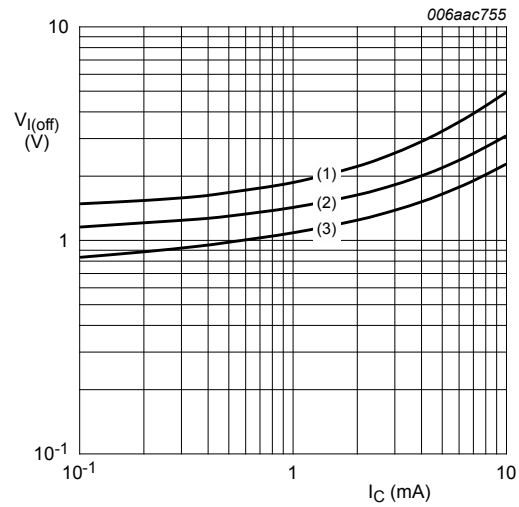
[1] Characteristics of built-in transistor





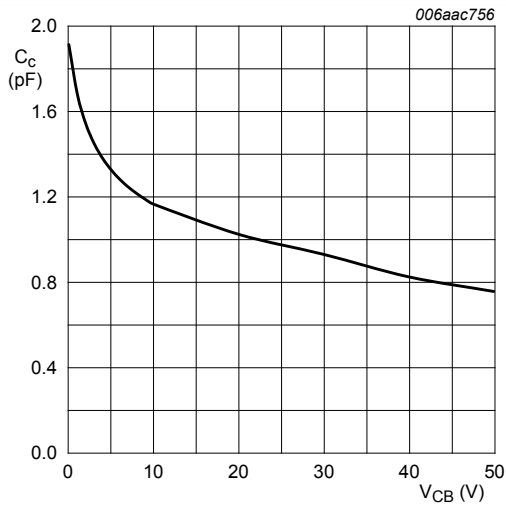
$V_{CE} = 0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 6. NPN transistor: On-state input voltage as a function of collector current; typical values



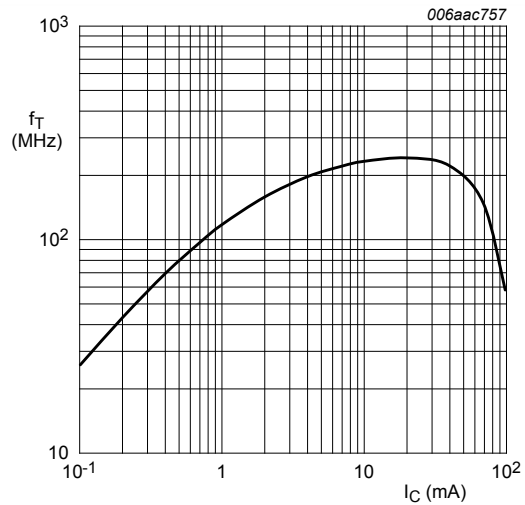
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 7. NPN transistor: Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 8. NPN transistor: Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = 5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 9. NPN transistor: Transition frequency as a function of collector current; typical values of built-in transistor

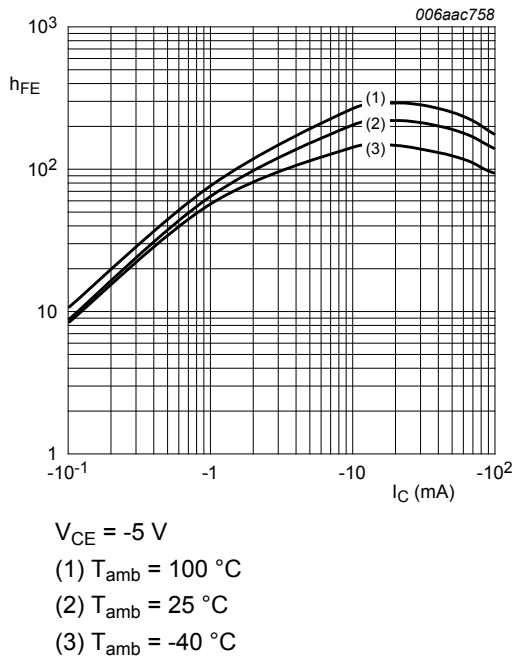


Fig. 10. PNP transistor: DC current gain as a function of collector current; typical values

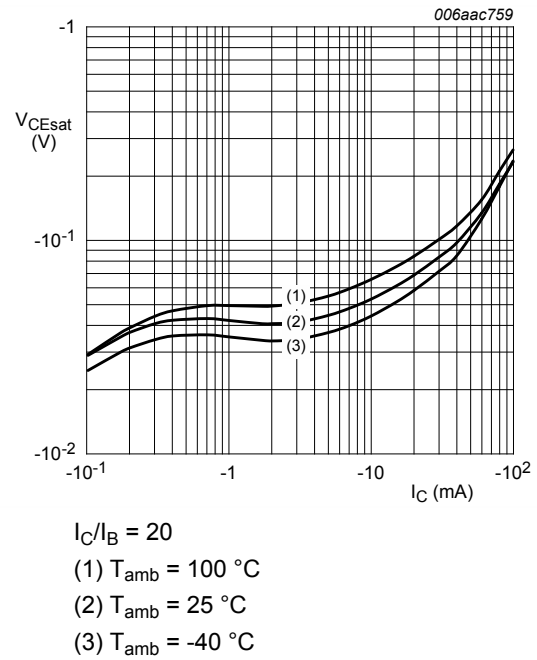


Fig. 11. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values

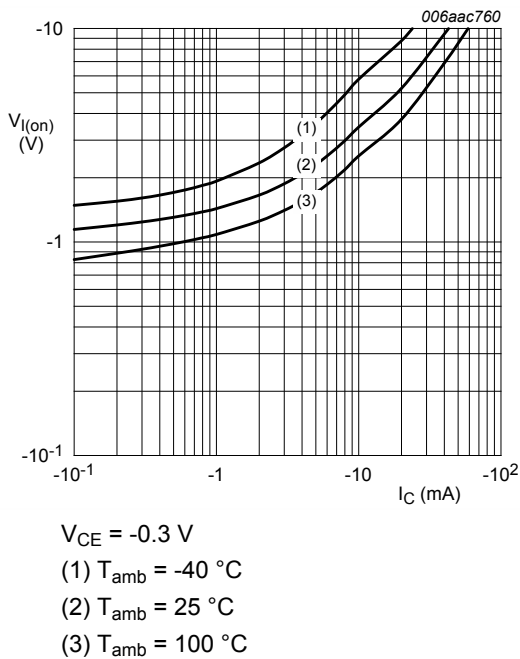


Fig. 12. PNP transistor: On-state input voltage as a function of collector current; typical values

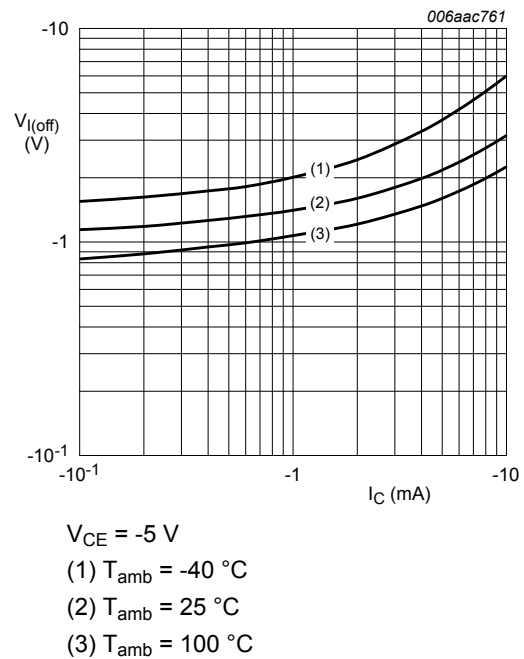


Fig. 13. PNP transistor: Off-state input voltage as a function of collector current; typical values

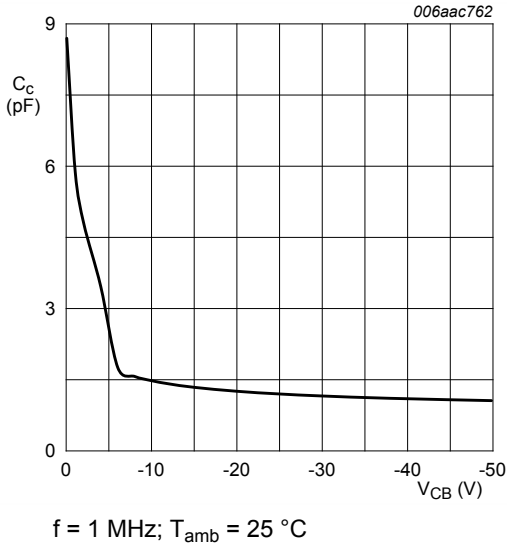


Fig. 14. PNP transistor: Collector capacitance as a function of collector-base voltage; typical values of built-in transistor

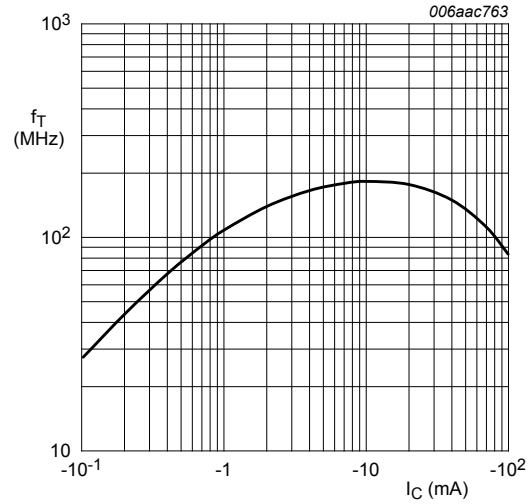


Fig. 15. PNP transistor: Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

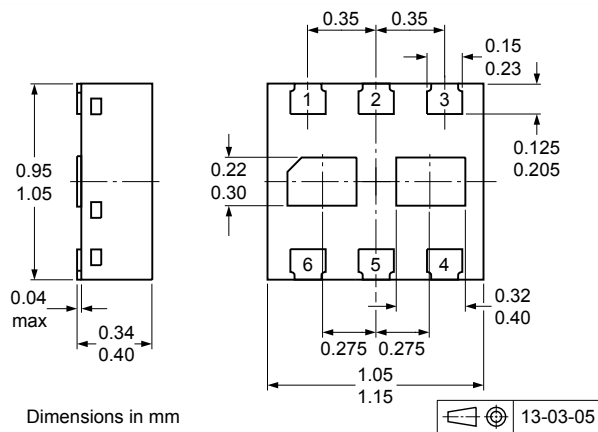


Fig. 16. Package outline DFN1010B-6 (SOT1216)

13. Soldering

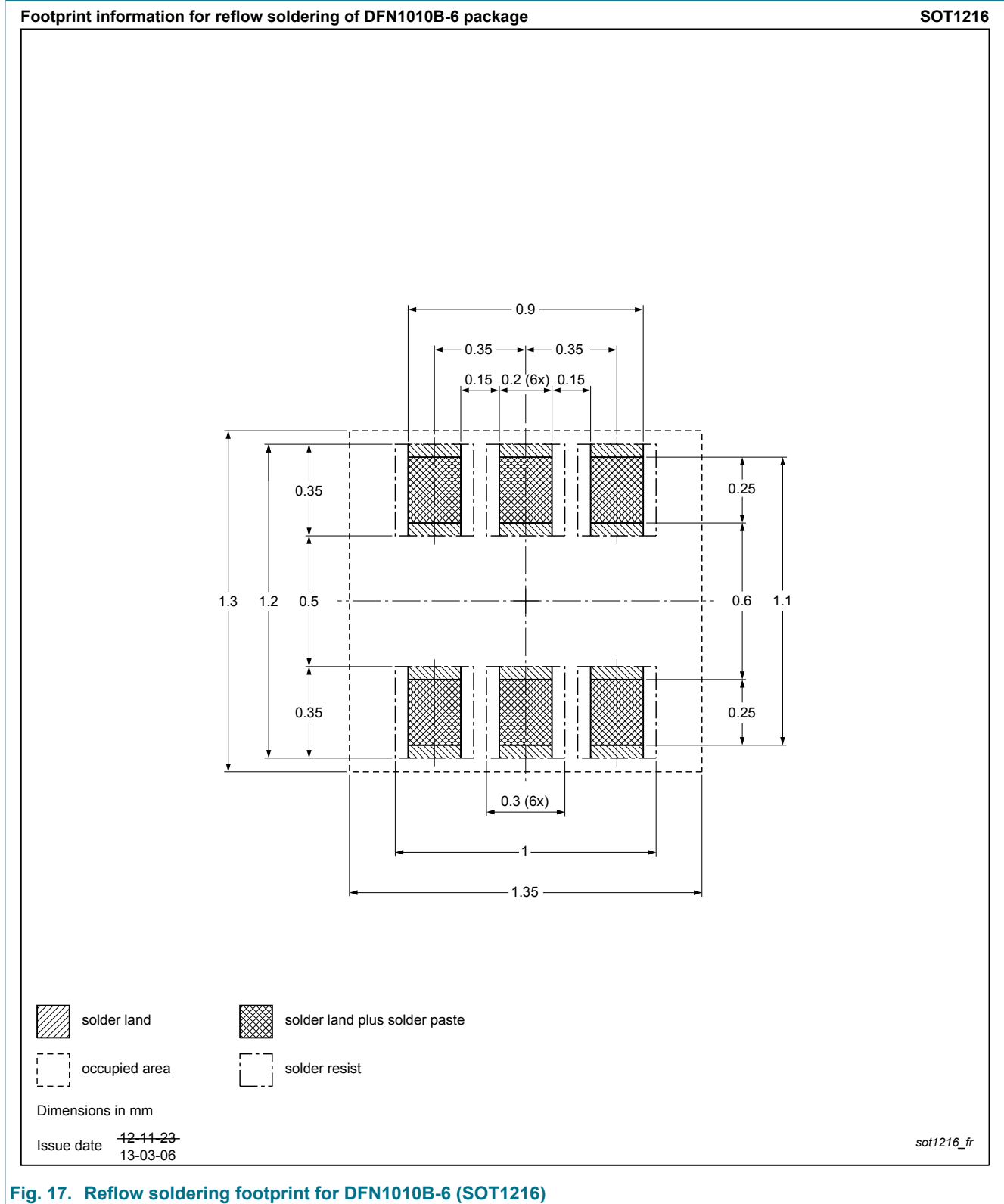


Fig. 17. Reflow soldering footprint for DFN1010B-6 (SOT1216)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PQMD12 v.1	20130724	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 24 July 2013